Hall Ticket Number:

Code No. : 31024 O2

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.C.A. I-Semester Backlog Examinations, Dec.-2018/Jan.-2019

Computer Organization

Time: 3 hours Max. Marks: 60

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. What is the purpose of Boolean Algebra?
2. How is overflow condition detected? Give an example.
3. Illustrate shift operations.
4. List various memory reference instructions.
5. List different Instruction formats.
6. Show the Mapping process of Instruction Code to Microinstruction address.
7. List major characteristics of RISC.
8. Define Assembler.
9. Illustrate handshaking in Asynchronous data transfer.
10. Define Page Fault.

Part-B (5 × 8 = 40 Marks)

11. a) Simplify using 3-Variable maps: $F(x,y,z) = \sum(3,4,6,7)$ [5]
    b) Show how Decoders with enable inputs can be connected to form a large Decoder? [3]
12. a) Develop 4-bit Arithmetic Circuit that can perform various arithmetic micro-operations. Give its function table. [3]
    b) Draw and explain Instruction cycle. [5]
13. a) Explain micro-programmed control organization with diagram. [4]
    b) Draw the flow chart for the first pass of the 2-pass assembler. [4]
14. a) Explain Addressing Modes with example. [5]
    b) Write short notes on pipelining. [3]
15. a) Discuss the Memory hierarchy. [5]
    b) Solve the given problem: If Address space is 16k, Memory space is 8k and page size is 1k. What is the logical address size (page number size and line number size) and physical address size (block number size and line number size)? How many pages can be accommodated in main memory and what is the size of page table and how many pages will have presence bit as 1? [3]
16. a) Explain different Flip-Flops. [4]
    b) Illustrate the Interrupt cycle with the help of flow chart. [4]
17. Answer any ***two*** of the following:
    a) Draw and explain the Micro-program sequencer. [4]
    b) Explain Booth's algorithm with example. [4]
    c) Illustrate DMA transfer in a computer system. [4]

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